Amendments to the Claims:

1. (original) A method for accessing a memory having a storage space larger than the addressing capability of a microprocessor, the memory comprising a plurality of memory banks, the microprocessor comprising a stack, an interrupt processing unit, and a memory bank selector for selecting the memory banks, the method comprising:

(a) storing an interrupt service routine in one of the memory banks;

(b) when an interrupt occurs, pushing a current program counter address onto the stack by the interrupt processing unit, pushing a bank number of the current memory bank onto the stack, and setting the memory bank selector to the bank number of the memory bank storing the interrupt service routine;

(c) switching the microprocessor to the memory bank storing the interrupt service routine to execute the interrupt service routine;

(d) after interrupt service routine finishes execution, popping the bank number of the memory bank stored in the stack in step (b) from the stack by the interrupt processor unit, restoring the popped bank number to the memory bank selector, and popping the program counter address stored in the stack in step (b) from the stack; and

(e) switching the microprocessor back to the memory bank corresponding to the bank number stored in the memory bank selector to continue executing the program interrupted in step (b).

2. (original) The method of claim 1 wherein the microprocessor is a MCS series microprocessor.

3. (original) The method of claim 1 wherein the method further comprises storing a common area in each memory bank.

4. (original) The method of claim 3 wherein the common area does not comprise the interrupt service routine.

5. (original) A single chip microprocessor for executing the method of claim 1.

6. (new) A device for increasing a storage capacity of a circuit, the device comprising:
a microprocessor for performing device operations according to a program code;
a memory unit coupled to the microprocessor, the memory unit comprising a plurality of memory banks for providing storage to the microprocessor;
wherein upon an interrupt, the microprocessor is for performing an interrupt service according to an interrupt service routine program stored in one of the memory banks, and the microprocessor is further for switching to the memory bank storing the interrupt service routine program to perform the interrupt service, and upon completion of the interrupt service routine, the microprocessor is for switching to a previous memory bank to resume performing the program code.

7. (new) The device of claim 6, wherein the microprocessor is further for pushing onto a stack a current program counter address and a bank number of a current memory bank upon the interrupt, and upon completion of the interrupt, the microprocessor is for popping from the stack the current program counter address and the bank number in order to switch to the previous memory bank and resume performing the program code.

8. (new) The device of claim 6, wherein the microprocessor is a MCS series microprocessor.